and the ID[7:0]# is driven on the bus to indicate the beginning of the Deferred phase. The next ordered transaction may begin at T7 although the current transaction is being deferred because VSBL# has been asserted at T5 indicating that visibility is guaranteed.

At T7, the Request phase of the next ordered transaction begins with the assertion of ADS# and request information being driven on the bus.

The visibility indication therefore avoids the delay caused by the waiting time from the deferred phase or deferred response.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as other embodiments of the invention, which are apparent to persons skilled in the art to which the invention pertains are deemed to lie within the spirit and scope of the invention.

What is claimed is:

1. A method for efficient memory access in a computer system that includes an agent coupled to a chipset via a bus, the method comprising:

issuing a first ordered transaction on the bus;

deferring processing of the first ordered transaction;

asserting a visibility signal by the chipset; and

issuing a second ordered transaction on the bus responsive to the visibility signal before the first ordered transaction is completed.

2. The method of claim 1 wherein the step of deferring comprises postponing the second ordered transaction if the visibility signal is negated.

3. The method of claim 1 further comprises stalling the first ordered transaction if the first ordered transaction is not ready.

4. The method of claim 1 further comprises accessing a cache line in a cache memory which is coupled to the bus if the cache line is one of the clean, shared, and modified states.

5. The method of claim 3 further comprises postponing the second ordered transaction until the first ordered transaction is complete.

6. The method of claim 4 further comprises completing the first ordered transaction.

7. A system comprising:

a bus;

a chipset coupled to the bus, the chipset being configured to generate a defer signal and a visibility signal; and an agent coupled to the bus and the chipset, wherein the agent is configured to:

(I) issue a first ordered transaction on the bus; (ii) defer processing the first ordered transaction in response to the defer signal; (iii) issue a second ordered transaction on the bus in response to the visibility signal before the first ordered transaction is complete.

8. The system of claim 7 wherein the agent postpones the second ordered transaction if the defer signal is asserted and the visibility signal is negated.

9. The system of claim 7 wherein the agent issues the second transaction if the defer signal is asserted and the visibility signal is asserted.

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